IN THE CLAIMS

1. (original) A power amplifier comprising:

a first switching device connected between a first supply voltage and a first output node;

a second switching device connected between a second supply voltage and a second output node; and

an inductance coupled between the first and second output nodes.

2. (original) The power amplifier of claim 1, wherein a load is coupled to the second output node.

3. (original) The power amplifier of claim 1, further comprising a first capacitor coupled to the first output node, and a second capacitor coupled to the second output node.

4. (original) The power amplifier of claim 1, further comprising a first capacitor coupled to the first output node.

5. (original) The power amplifier of claim 1, further comprising a first capacitor coupled between the first and second output nodes.

6. (original) The power amplifier of claim 1, wherein the first and second switching devices are driven by signals that repeatedly turn the devices on and off.

7. (original) The power amplifier of claim 6, wherein the first and second switching devices are both cycled on during the same time period, and wherein the first and second switching devices are both cycled off during the same time period.

8. (original) The power amplifier of claim 4, wherein the first capacitor is provided by the input capacitance of a third switching device.

9. (original) The power amplifier of claim 3, wherein the first capacitor is provided by the input capacitance of a third switching device, and wherein the second capacitor is provided by the input capacitance of a fourth switching device.

10. (original) The power amplifier of claim 1, wherein the first and second switching devices are comprised of transistors.

11. (original) The power amplifier of claim 1, wherein the first switching device is comprised of a PMOS transistor, and wherein the second switching device is comprised of an NMOS transistor.

12. (original) The power amplifier of claim 1, further comprising a load coupled across the first and second output nodes.

13. (original) The power amplifier of claim 1, further comprising a transformation network coupled to the first and second output nodes.

14. (original) The power amplifier of claim 13, wherein the transformation network further comprises:

a capacitor coupled to the first output node and a third node;

an inductor coupled to the second output node and the third node; and

a load coupled to the third node.

15. (original) The power amplifier of claim 1, further comprising a preamplifier connected to the power amplifier, the preamplifier further comprising:

a third switching device connected between said first supply voltage and a third node and coupled to the input to the first switching device;

a fourth switching device connected between said second supply voltage and a fourth node and coupled to the input to the second switching device; and

a second inductor coupled between the third and fourth nodes.

16. (original) The power amplifier of claim 1, further comprising one or more inductors coupled between the first output node and a third supply voltage.

17. (original) The power amplifier of claim 1, further comprising one or more inductors coupled between the first output node and a third supply voltage, and one or more inductors coupled between the second output node and a fourth supply voltage.

18. (original) A method of reducing the peak output voltage of an amplifier comprising the steps of:

providing an inductor having first and second terminals;

providing a first switching device connected between the first terminal of the inductor and a first supply voltage;

providing a second switching device connected between the second terminal of the inductor and a second supply voltage;

applying a voltage between the first and second terminals of the inductor during a first portion of a clock cycle by turning on the first and second switching devices; and

turning off the first and second switching devices during a second portion of the clock cycle.

19. (original) The method of claim 18, further comprising the steps of providing a first capacitance connected to the first terminal, providing a second capacitance connected to the second terminal, wherein current from the inductor charges or discharges the first and second capacitances during the second portion of the clock cycle.

20. (original) The method of claim 18, further comprising the step of connecting a load to the first node.

Claims 21-46 (canceled)